

HD14536B

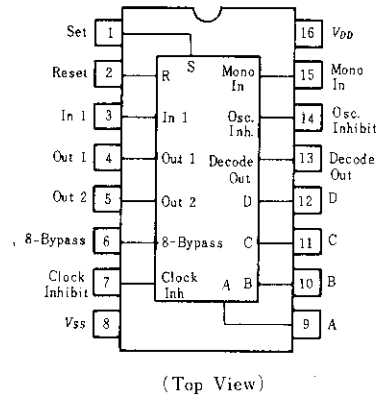
Programmable Timer

The HD14536B programmable timer is a flexible 24-stage ripple binary counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing can be achieved.

FEATURES

- 24 Flip-Flop Stages ... Will Count from 2^0 to 2^{24}
- Last 16 Stages Selectable by Four-Bit Select Code
- Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit Input
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation with Very Long Rise and Fall Times
- Clock Input $f_{max} = 3\text{MHz typ. @}10\text{V}$
- Counter Advances On Negative Going Edge of Clock
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

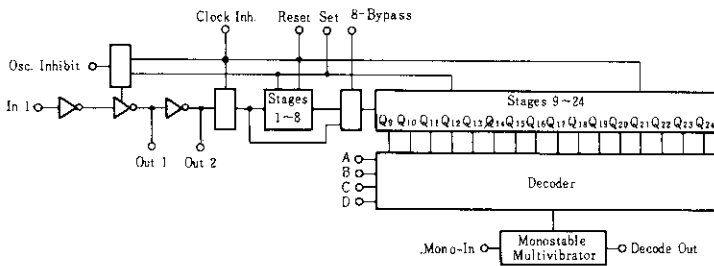
PIN ARRANGEMENT



TRUTH TABLE

D	C	B	A	Decode Out	8-Bypass
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

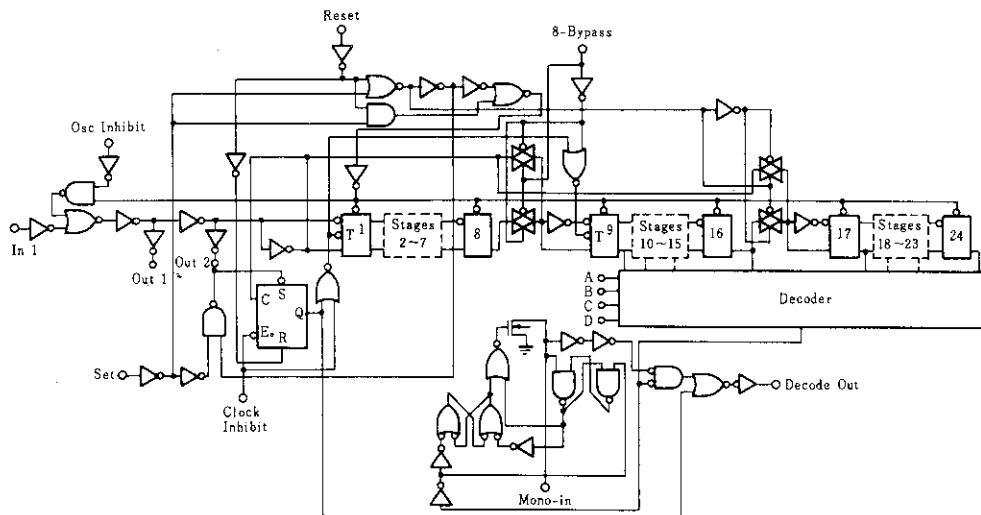
BLOCK DIAGRAM



In 1	Set	Reset	Clock Inhibit	Osc. Inhibit	Out 1	Out 2	Decode Out
	0	0	0	0			No Change
	0	0	0	0			Advance to next stage
x	1	0	0	0	0	1	1
x	0	1	0	0	0	1	0
x	0	0	1	0			No Change
0	0	0	0	x	0	1	No Change
1	0	0	0				Advance to next stage

x Don't Care

LOGIC DIAGRAM



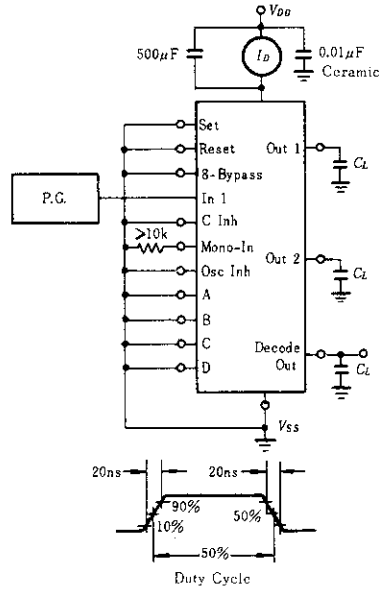
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit
			min	max	min	typ	max	min	max	
Output Voltage	V_{OL}	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
			—	0.05	—	0	0.05	—	0.05	
			—	0.05	—	0	0.05	—	0.05	
	V_{OH}	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
			9.95	—	9.95	10	—	9.95	—	
			14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	$V_{out}=4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{out}=9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0	
		$V_{out}=13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	$V_{out}=0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V
		$V_{out}=1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—	
		$V_{out}=1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	$V_{OH}=2.5V$	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		$V_{OH}=4.6V$	-0.2	—	-0.16	-0.36	—	-0.12	—	
		$V_{OH}=9.5V$	-0.5	—	-0.4	-0.9	—	-0.3	—	
	I_{OL}	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—	
		$V_{OL}=1.5V$	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.3	—	± 0.0001	± 0.3	—	± 1.0	μA
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	Zero Signal, per Package	—	50	—	0.010	50	—	375	μA
			—	100	—	0.020	100	—	750	
			—	200	—	0.030	200	—	1500	
Total Supply Current*	I_T	Dynamic + I_{DD} , per Gate	—	—	—	1.15	—	—	—	μA
			—	—	—	2.3	—	—	—	
		$C_L=50pF$, $f=1kHz$	—	—	—	3.55	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

@ $V_{DD}=5.0V$ $I_T=(1.15\mu A/kHz)f+I_{DD}$, @ $V_{DD}=10V$ $I_T=(2.3\mu A/kHz)f+I_{DD}$, @ $V_{DD}=15V$ $I_T=(3.55\mu A/kHz)f+I_{DD}$

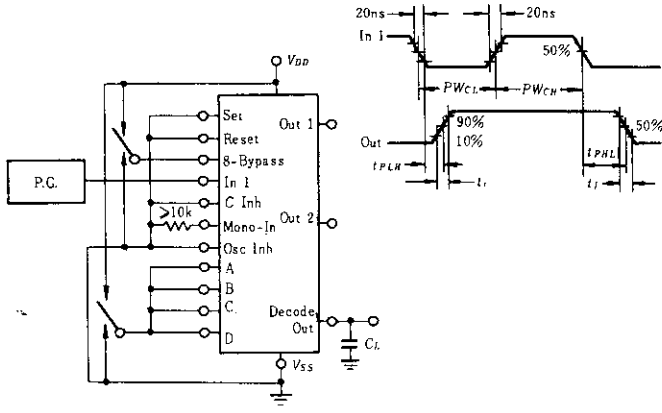
●POWER DISSIPATION TEST
CIRCUIT AND WAVEFORM

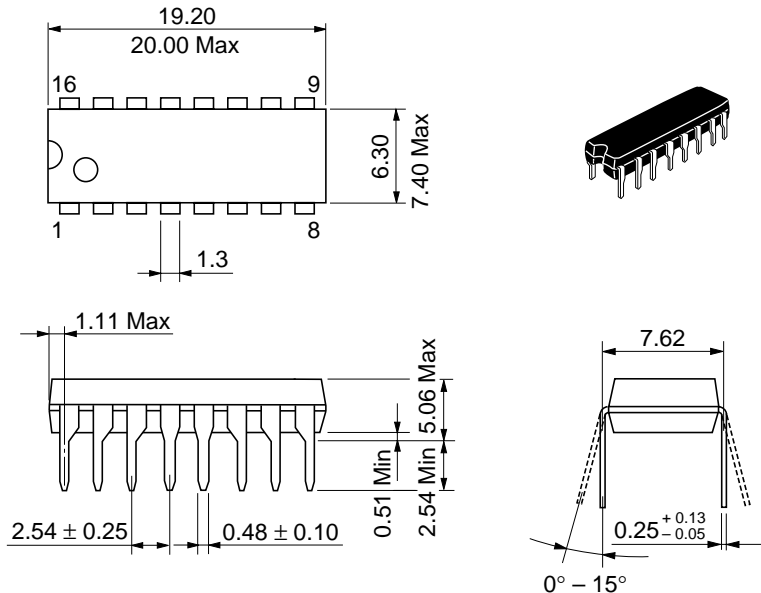


■ SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

Characteristic		Symbol	$V_{DD}(V)$	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	120	250	ns
			10	—	60	125	
			15	—	40	100	
Propagation Delay Time	Clock to Q_1 (Pin 6 High)	t_{PLH}	5.0	—	1800	5400	ns
			10	—	650	2000	
			15	—	450	1500	
	Clock to Q_1 (Pin 6 Low)	t_{PHL}	5.0	—	3.8	12	μs
			10	—	1.5	4.5	
			15	—	1.1	3.5	
		Clock to Q_{1s}	5.0	—	7.0	21	
			10	—	3.0	9.0	
			15	—	2.2	7.0	
	Reset to Q_n	t_{PHL}	5.0	—	1500	4500	ns
			10	—	600	1800	
			15	—	450	1400	
Clock Pulse Width		PW_C	5.0	900	300	—	ns
			10	300	100	—	
			15	255	85	—	
Clock Frequency		PRF	5.0	—	1.2	0.4	MHz
			10	—	3.0	1.5	
			15	—	5.0	2.0	
Clock Pulse Rise and Fall Time		t_r, t_f	5.0	No Limit			
			10				
			15				
Reset Pulse Width		PW_R	5.0	1500	500	—	ns
			10	600	200	—	
			15	450	150	—	

■ SWITCHING TIME TEST CIRCUIT





Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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